XFT Stereo Finder
Design Review

(FNAL)
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Project Overview

Stereo XFT Upgrade

- **add 3 stereo layers SL7, SL5,SL3**
- **L1 data path through "SLAM"**
- **New "Stereo" L2 data path**

System Overview

**Ansley trigger cable (220 ft)
Data @45MHz LVDS**

**~2 m copper Cable Data
@33MHz (channel link)**

**Neighboring cards
connected over backplane**

168 TDC from COT axial layers

XTC

24+24 Axial Finders

24 Linkers

24 SLAMs

24 crates

3 crates

3 crates

~10 m of cable to XTRP

Additional optical output

New cable (~150ft) Optical Data ~62.5MHz

New TDC or XTC for stereo layers

12+12+12 Stereo Finders

~3m optical Cable @62.5MHz

2 crates

Data to L2

Stereo Implementation

Stereo Finder

- **Plan to instrument SL3,SL5, and SL7**

- **Each Finder will cover a 30˚ section**

  Each SL will require 12 Stereo Finders, for a total of 36 production boards.
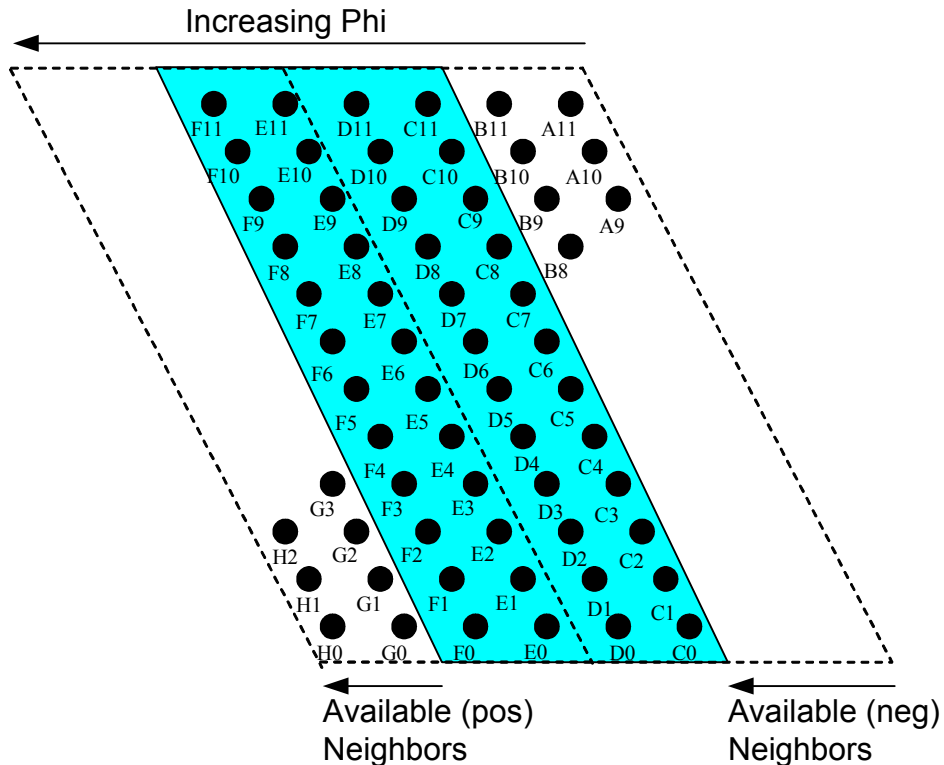
Finder Inputs

A Finder "cell" is defined as a group of 12 TDC wires.

Previous Finder algorithms worked off a "core" of 4 cells plus neighbors.

**4 cells represent data from 48 wires, or half a TDC.**

Increasing Phi

F11 E11 D11 C11 B11 A11
F10 E10 D10 C10 B10 A10
F9 E9 D9 C9 B9 A9
F8 E8 D8 C8 B8
F7 E7 D7 C7
F6 E6 D6 C6
F5 E5 D5 C5
F4 E4 D4 C4
G3 F3 E3 D3 C3
H2 G2 F2 E2 D2 C2
H1 G1 F1 E1 D1 C1
H0 G0 F0 E0 D0 C0

Available (pos) Neighbors

Available (neg) Neighbors

Finder Algorithm

Finder Algorithm

- **similar to axial XFT**

- **utilizes mask sets to match possible tracks**

- **more details on this from Scott Holm**

Track Segment

+Neighbor
Ansley
Cable

Core
Ansley
Cable

- Neighbor
Ansley
Cable
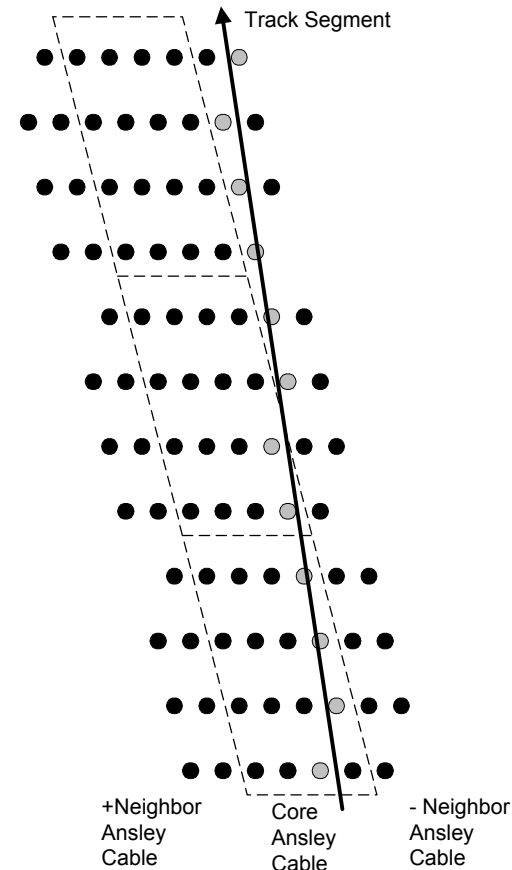
Gray Wires indicate 12 wire mask for the depicted track segment

Implementation

Finder algorithm is being implemented in an Altera EP2S60 FPGA. Each FPGA will handle 8 cells.

	# of Finder Cells in COT layer	# of 8 cell cores in COT layer	# of FPGAs required for 30˚ (Board)
SL7	432	54	4.5 -> 5
SL5	336	42	3.5 -> 4
SL3	240	30	2.5 -> 3

TDC Inputs

- **The source of the XFT data are TDC modules.**

- **These modules contain timing information for 96 wires.**

- **The TDC will produces 6 bits of data (6 time slices) for each wire.**

- **This data identifies whether a wire has a "hit" on it for a particular time slice.**

- **There are 6 identified time slices within each 396ns period, or 3 CDF_Clock cycles.**

In addition to sending up the hit information for each wire, it is desirable to tag the information with a Beam_Zero marker, to identify its position in time as well as some type of identification tag to mark the source of the data.

TDC Inputs

Plan is to send the data from the TDC modules to the XFT modules via an 8B/10B encoded serial optical bitstream.
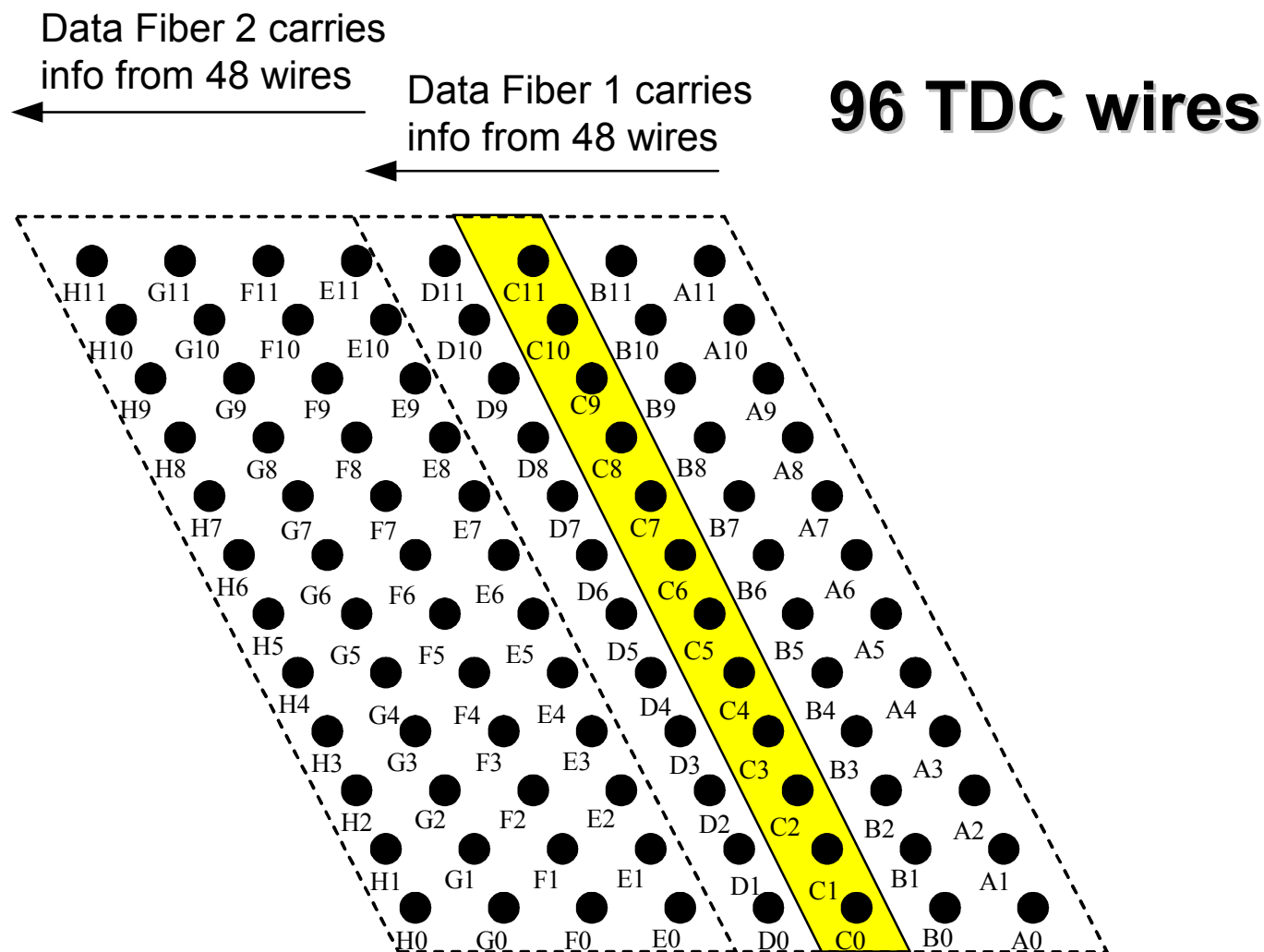
Furthermore, we will limit the data rate on such a link to ~1.25Gbps which is supported by a wide variety of commercial products available for Gigabit Ethernet.

TDC Data Representation

Data Fiber 2 carries info from 48 wires

Data Fiber 1 carries info from 48 wires

96 TDC wires

Data Packing using 16 bit Serializer

Data Fiber # 1 carries information from TDC wires 0-47

Data Word	Beam_Zero Marker 1 bit	Word Zero Flag 1 bit	Group Identifies 2 bits	Wire data time slice (0-5) 12 bits
1	beam_zero	1	00	t0 (A0-A11)
2	beam_zero	1	01	t0 (B0-B11)
3	beam_zero	1	10	t0 (C0-C11)
4	beam_zero	1	11	t0 (D0-D11)
5	beam_zero	0	00	t1 (A0-A11)
6	beam_zero	0	01	t1 (B0-B11)
7	beam_zero	0	10	t1 (C0-C11)
8	beam_zero	0	11	t1 (D0-D11)
9	beam_zero	0	00	t2 (A0-A11)
10	beam_zero	0	01	t2 (B0-B11)
11	beam_zero	0	10	t2 (C0-C11)
12	beam_zero	0	11	t2 (D0-D11)
13	beam_zero	0	00	t3 (A0-A11)
14	beam_zero	0	01	t3 (B0-B11)
15	beam_zero	0	10	t3 (C0-C11)
16	beam_zero	0	11	t3 (D0-D11)
17	beam_zero	0	00	t4 (A0-A11)
18	beam_zero	0	01	t4 (B0-B11)
19	beam_zero	0	10	t4 (C0-C11)
20	beam_zero	0	11	t4 (D0-D11)
21	beam_zero	0	00	t5 (A0-A11)
22	beam_zero	0	01	t5 (B0-B11)
23	beam_zero	0	10	t5 (C0-C11)
24	beam_zero	0	11	t5 (D0-D11)

If the data is packed as in the previous example,

We would need a data rate of:

20 encoded bits/16 data bits x 16 data bits x 24 words ÷ 396ns = 1.21 Gbps

This would require a Serdes clock period of 16.5 ns

(CDF_Clock ÷ 8)

The recommended clock jitter of the Serdes parts is ~40ps pk-pk. It would be very difficult to achieve this with detector clock. We may run the links with 62.500 MHz oscillator which is slightly faster (16ns clock period) than CDF_Clock ÷ 8.
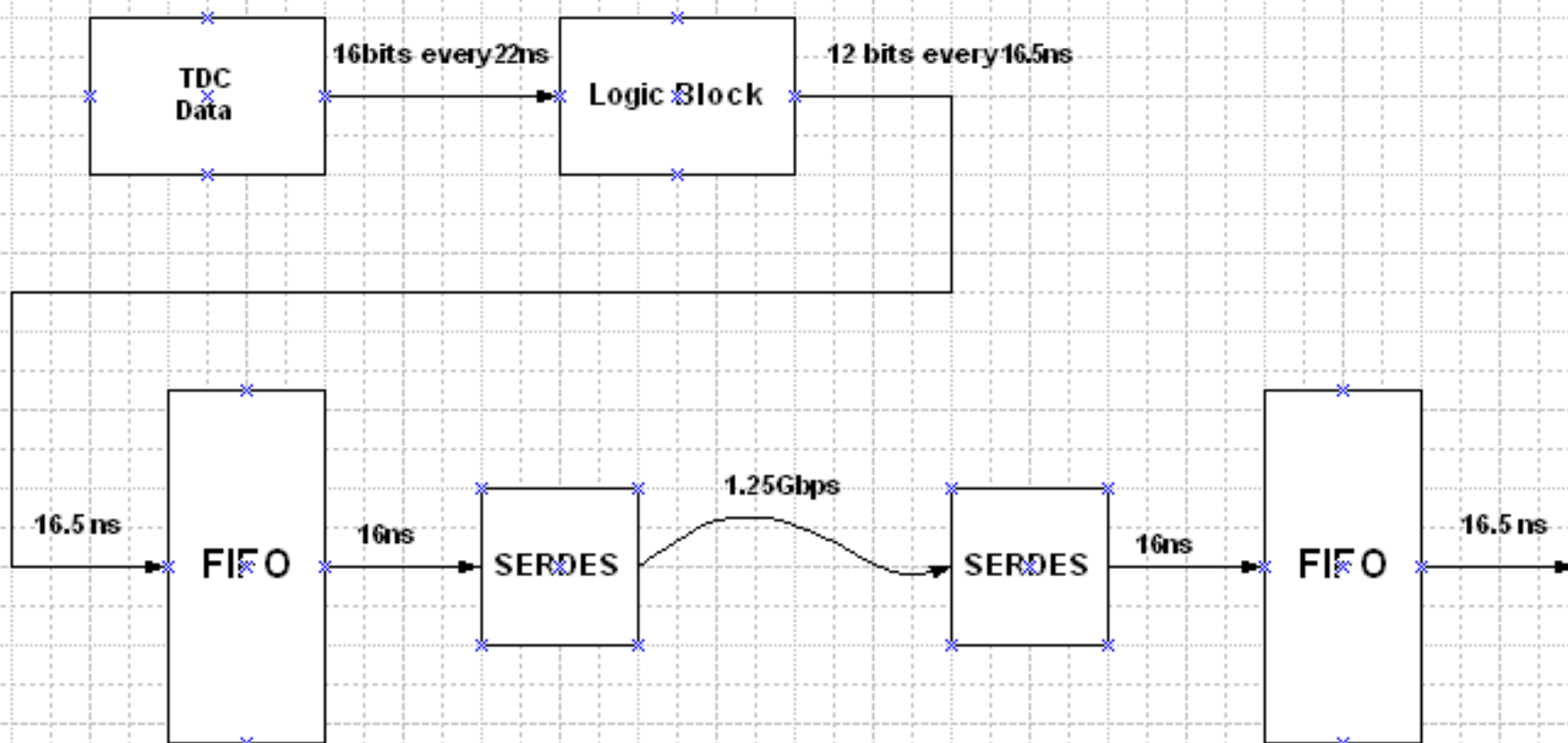
-> some kind of buffer/FIFO to smooth out clock differences

M2R-25-4-1-TL Optical Gigabit Ethernet/Fibre Channel
850nm SFF 2x5 Dual Receivers -- 1.25/1.0625GBaud --- +3.3V

Dual Receivers

Features
- 1.25 Gbps Gigabit Ethernet Compliant
- Metalized Plastic Package
- TTL Signal Detect output
- AC coupled PECL level outputs
- Low profile fits Mezzanine Card Applications
- Single +3.3V Power Supply
- Wave Solderable / Aqueous Washable
- Class 1 Laser Safety Compliant
- UL 1950 Approved

PRODUCT OVERVIEW
The M2R-25-4-1-TL Small Form Factor (SFF) optical dual receiver modules are high performance integrated duplex data links for uni-directional communication over multimodeoptical fibre. The M2R-25-4 module is

M2T-25-4-1-L Optical Gigabit Ethernet/Fibre Channel
850nm SFF LC 2x5 Dual Transmitters - 1.25/1.0625GBaud -- +3.3V

Dual Transmitters

Features
- 1.25 Gbps Gigabit Ethernet Compliant
- 1.0625Gbps Fibre Channel Compliant
- Metalized Plastic Package
- AC coupled PECL level Inputs
- Low profile fits Mezzanine Card Applications
- Single +3.3V Power Supply
- Wave Solderable / Aqueous Washable
- Class 1 Laser Safety Compliant
- UL 1950 Approved

PRODUCT OVERVIEW
The M2T-25-4-1-L Small Form Factor (SFF) optical dual transmitter modules are high performance integrated duplex data links for uni-directional communication over multimode optical fibre. The M2T-25-4 module is specifically designed to used in Gigabit Etherent/ Fibre

TLK1501
0.6 TO 1.5 GBPS TRANSCEIVER

SLLS428F – JUNE 2000 – REVISED JANUARY 2004

- Hot Plug Protection
- 0.6 to 1.5 Gigabits Per Second (Gbps) Serializer/Deserializer
- High-Performance 64-Pin VQFP Thermally Enhanced Package (PowerPAD™)
- 2.5 V Power Supply for Low Power Operation
- Programmable Voltage Output Swing on Serial Output
- Interfaces to Backplane, Copper Cables, or Optical Converters
- Rated for Industrial Temperature Range

- On-Chip 8-Bit/10-Bit (8B/10B) Encoding/Decoding, Comma Alignment, and Link Synchronization
- On-Chip PLL Provides Clock Synthesis From Low-Speed Reference
- Receiver Differential Input Thresholds 200 mV Minimum
- Typical Power: 250 mW
- Loss of Signal (LOS) Detection
- Ideal for High-Speed Backplane Interconnect and Point-to-Point Data Link

Optical Mezzanine Cards

Two types of optical Mezzanine Cards will be used on the Stereo XFT
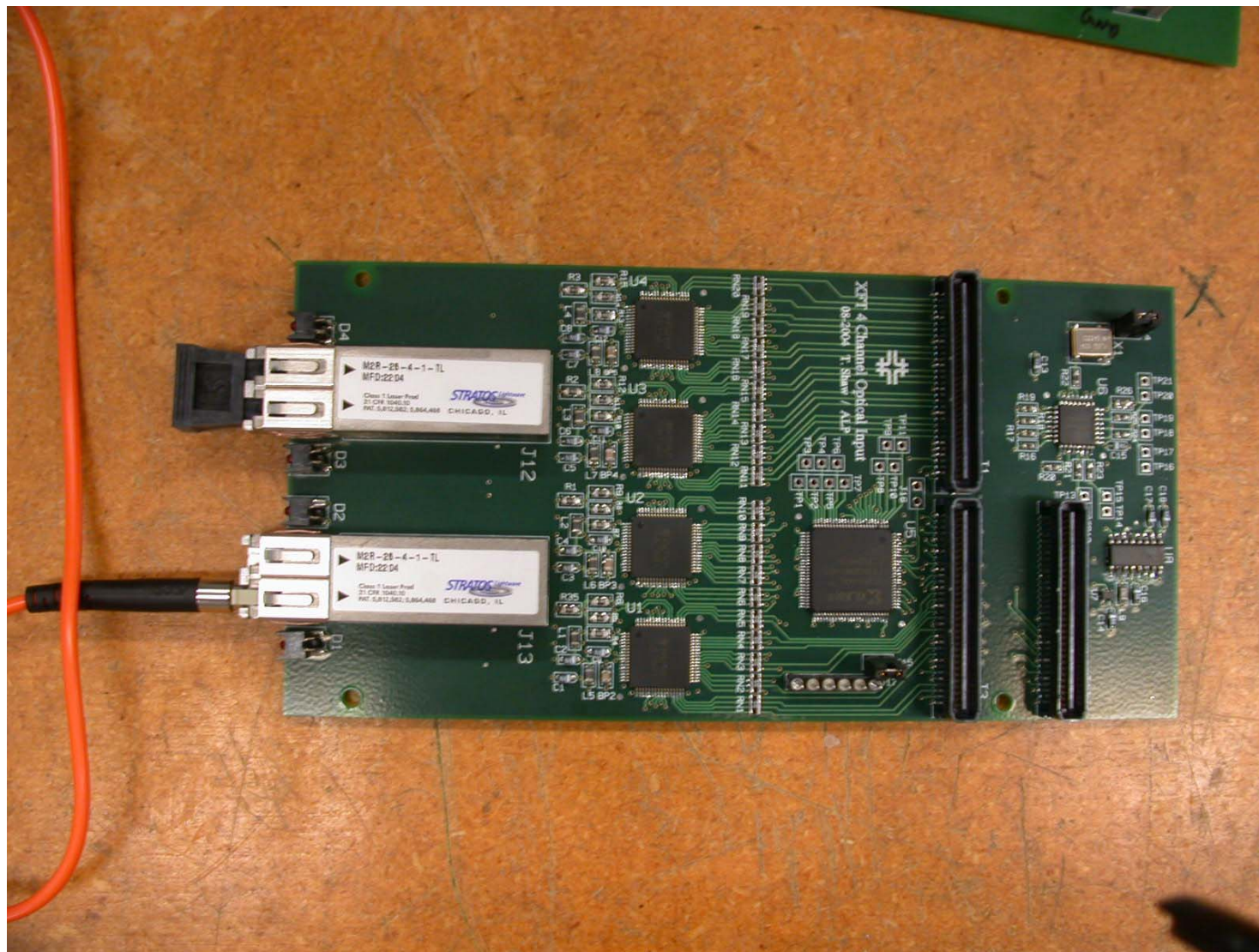
- A four channel Receiver Module (RX_MEZZ) to receive the TDC data

- A four (six?) channel Transmitter Module (TX_MEZZ) to drive data to the SLAM
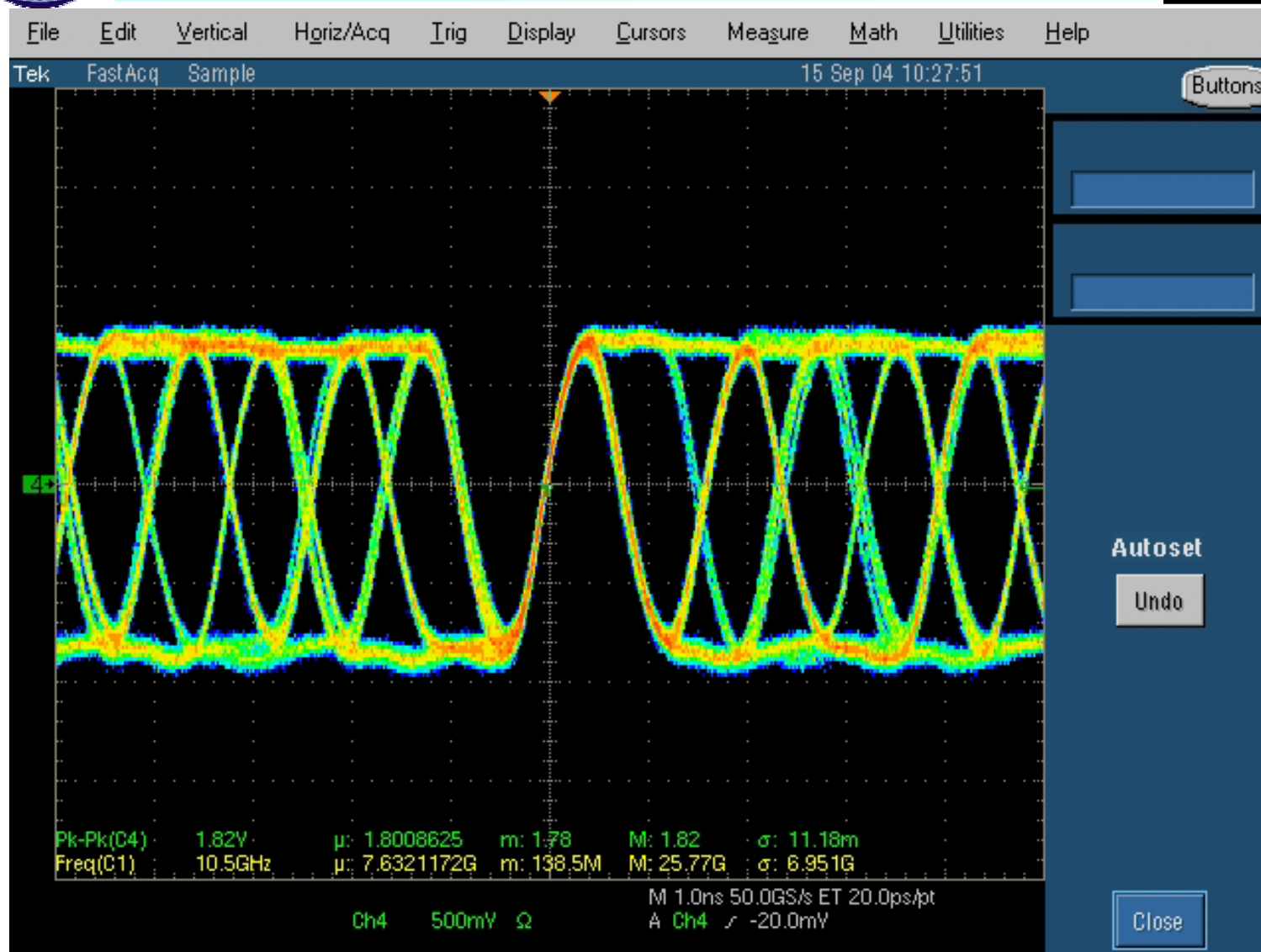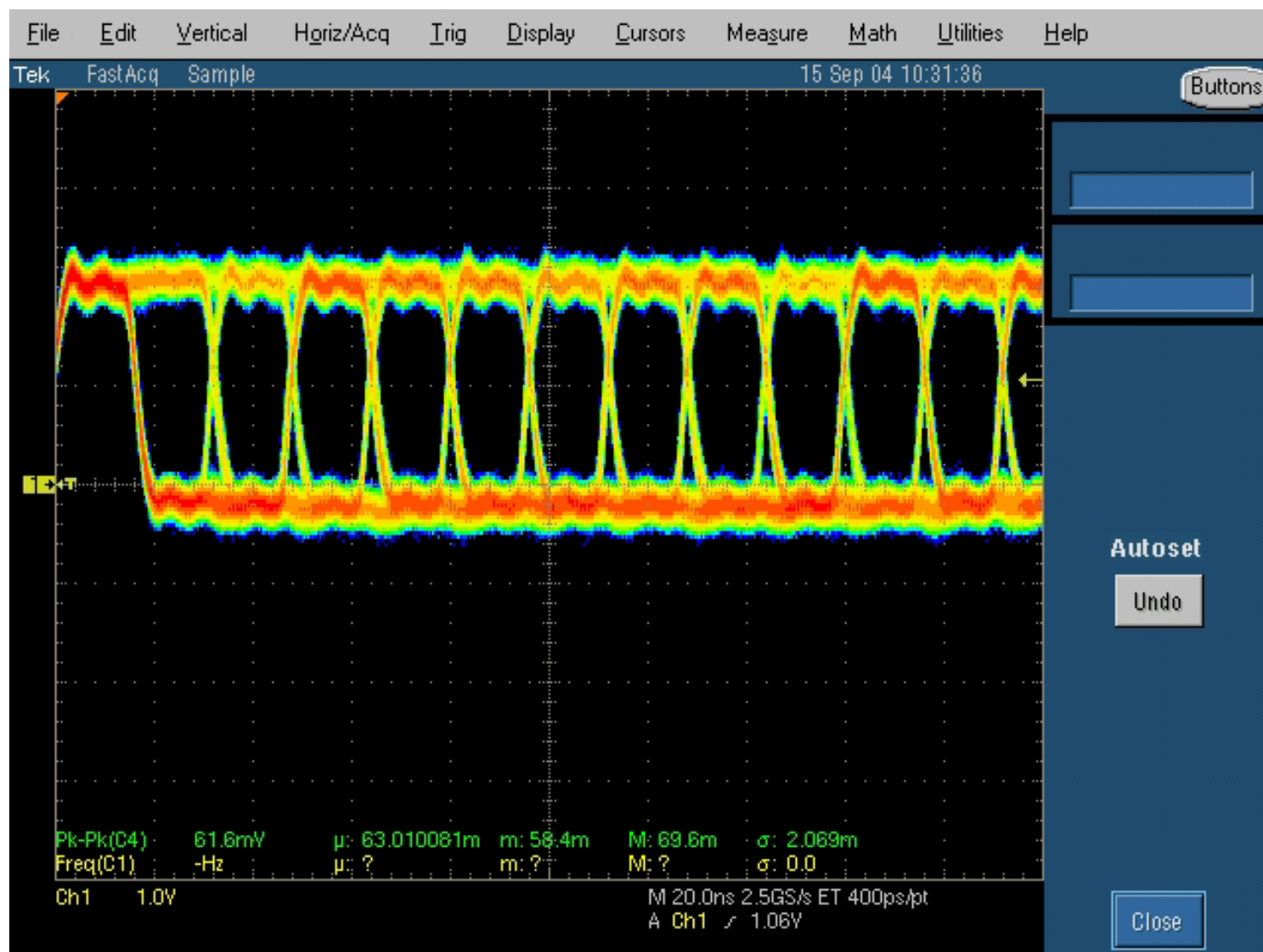
RX Mezzanine

Serial Input data - Electrical

Deserialized Data

Finder Outputs

Stereo Finders will output data to L2 and SLAM boards. SLAM boards will provide inputs to XTRP.

L2 output estimated to be ~120 bytes per board. We will use a serial optical link utilizing 8B/10B format. The data will be sent to a Pulsar Card which uses the TX_Mezz.

SLAM output requires 12bits/cell for each Finder Module. This link will use fiber optic technology similar to TDC->Finder links.

SLAM Data Format

Data Word	Beam_Zero Marker 1 bit	Start Event Flag 1 bit	End Event Flag 1 bits	Error Flag 1 bit	Pixel data 12 bits
1	beam_zero	1	0	error	1st cell data(11:0)
2	beam_zero	0	0	error	cell data(11:0)
3	beam_zero	0	0	error	cell data(11:0)
4	beam_zero	0	0	error	cell data(11:0)
…	beam_zero	0	0	error	cell data(11:0)
N-1	beam_zero	0	0	error	cell data(11:0)
N	beam_zero	0	1	error	last cell data(11:0)

Posible Data Transmission Format between Stereo Finder and the SLAM
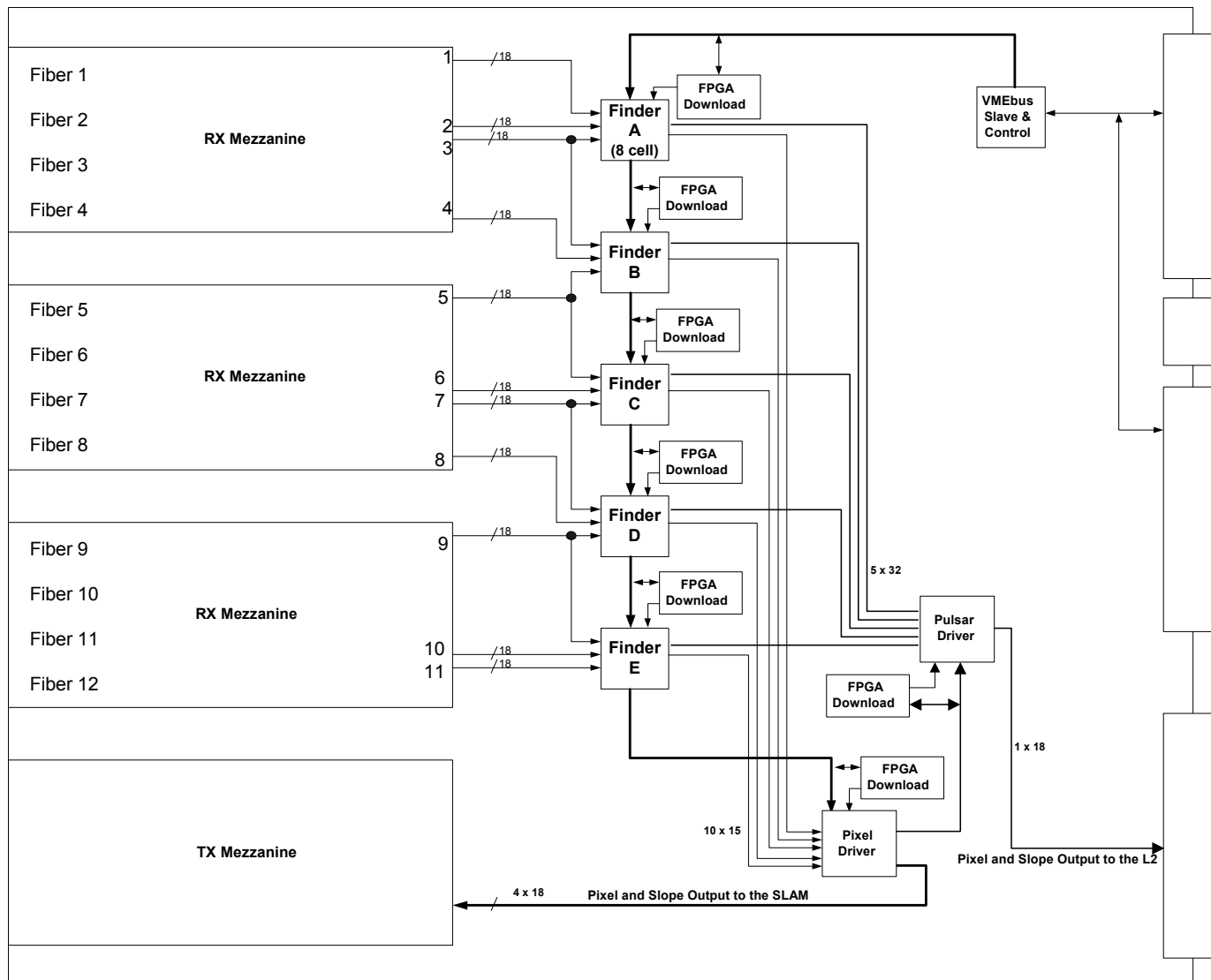
FPGA Download

There are 8 EP2S60 FPGAs on each board

- **Finder FPGAs (Qty 5)**

  Downloadable via

  - **JTAG**
  - **One of two Altera Configuration Devices (writeable Flash memory via VME or JTAG)**

- **Pixel Driver FPGA (SLAM output) (Qty 1)**

  Downloadable via

  - **JTAG**
  - **One of two Altera Configuration Devices (writeable Flash memory via VME or JTAG)**

- **L2 Output FPGA (Qty 1)**

  Downloadable via

  - **JTAG**
  - **One of two Altera Configuration Devices (writeable Flash memory via VME or JTAG)**

- **VMEbus Interface FPGAs (Qty 5)**

  Downloadable via

  - **JTAG**
  - **One Altera Configuration Devices (writeable Flash memory via JTAG)**

Power requirements are summarized in the table below. DC-DC converters will be used to generate the +3.3V, +2.5V and +1.2V power rails. The +3.3V rail is generated by a Datel UNR-3.3/20-D5 DC-DC converter which is capable of delivering up to 20Amps of 3.3V.
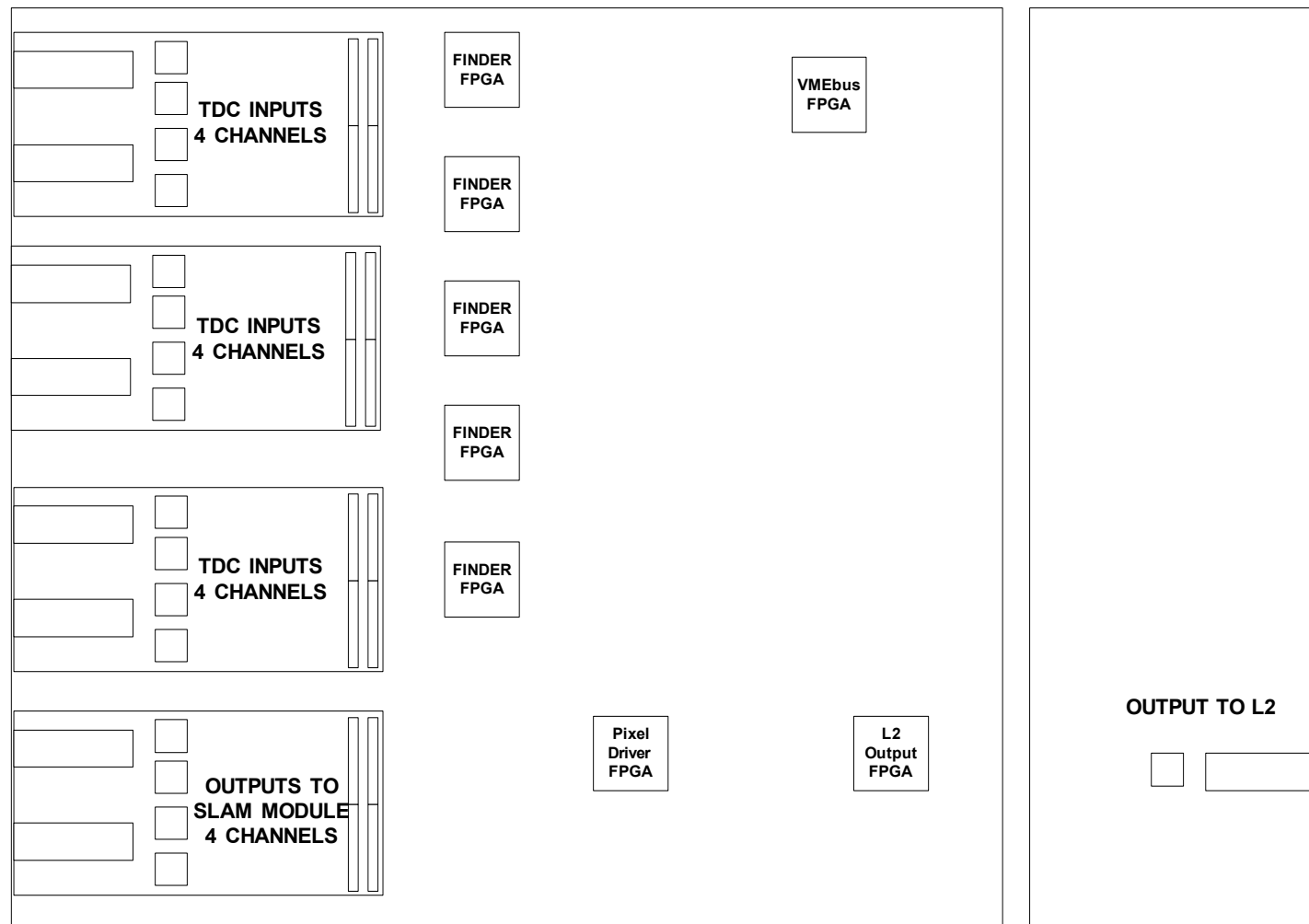
+2.5V and +1.2V are produced by Datel's LSM-2.5/10-D3 and LSM-1.2/10-D3 respectively. Each of these is capable of providing up to 10Amps is uses the +3.3V rail for conversion.

Power Rail	Estimated Power (W)
+5V	0.5
+3.3V	15.2
+2.5V	6.6
+1.2V	4.9

FINDER FPGA

FINDER FPGA

FINDER FPGA

FINDER FPGA

FINDER FPGA

VMEbus FPGA

TDC INPUTS 4 CHANNELS

TDC INPUTS 4 CHANNELS

TDC INPUTS 4 CHANNELS

OUTPUTS TO SLAM MODULE 4 CHANNELS

Pixel Driver FPGA

L2 Output FPGA

OUTPUT TO L2

9U x 400mm Main Module

Transition Module
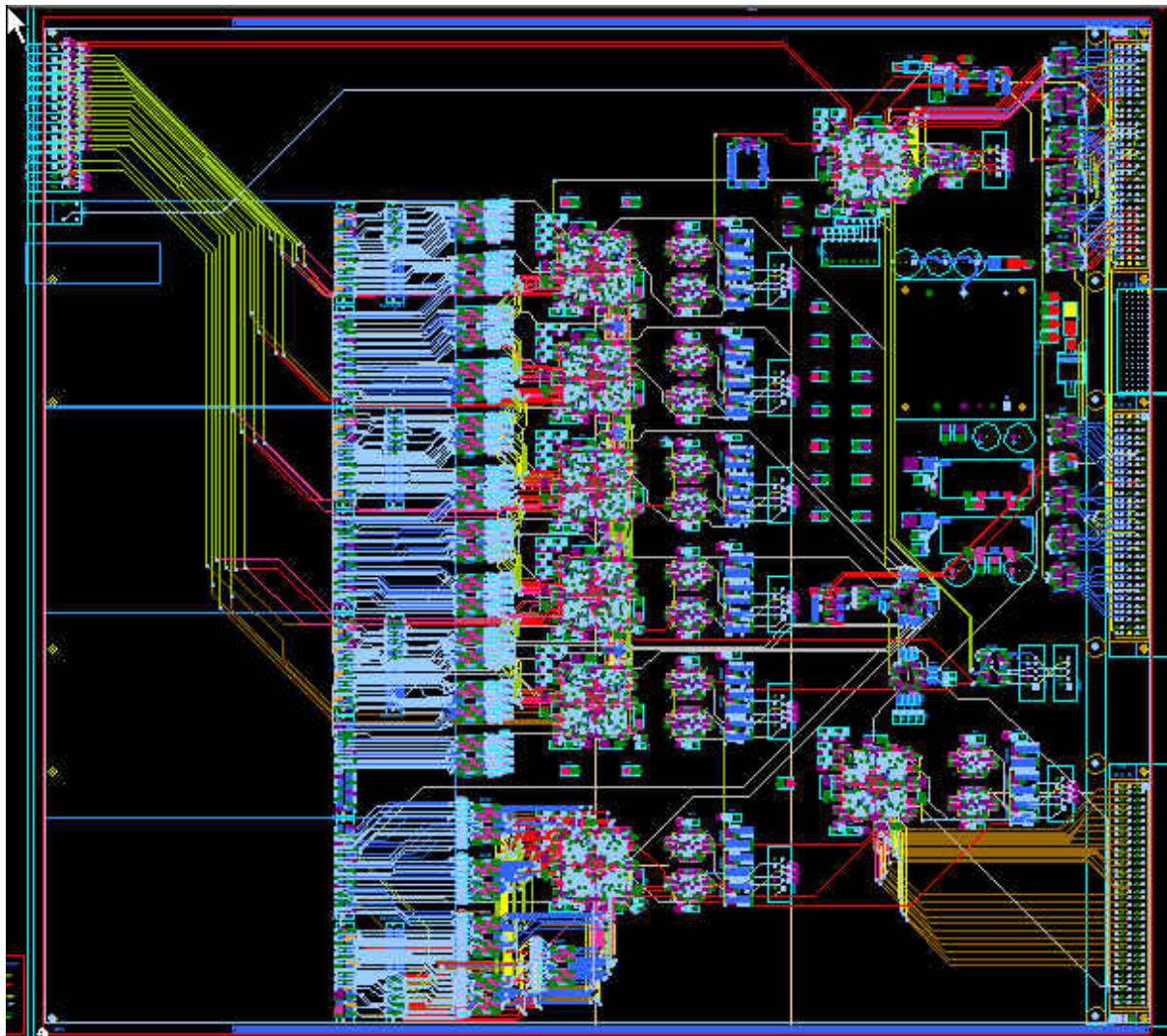
XFT Stereo Layout -2
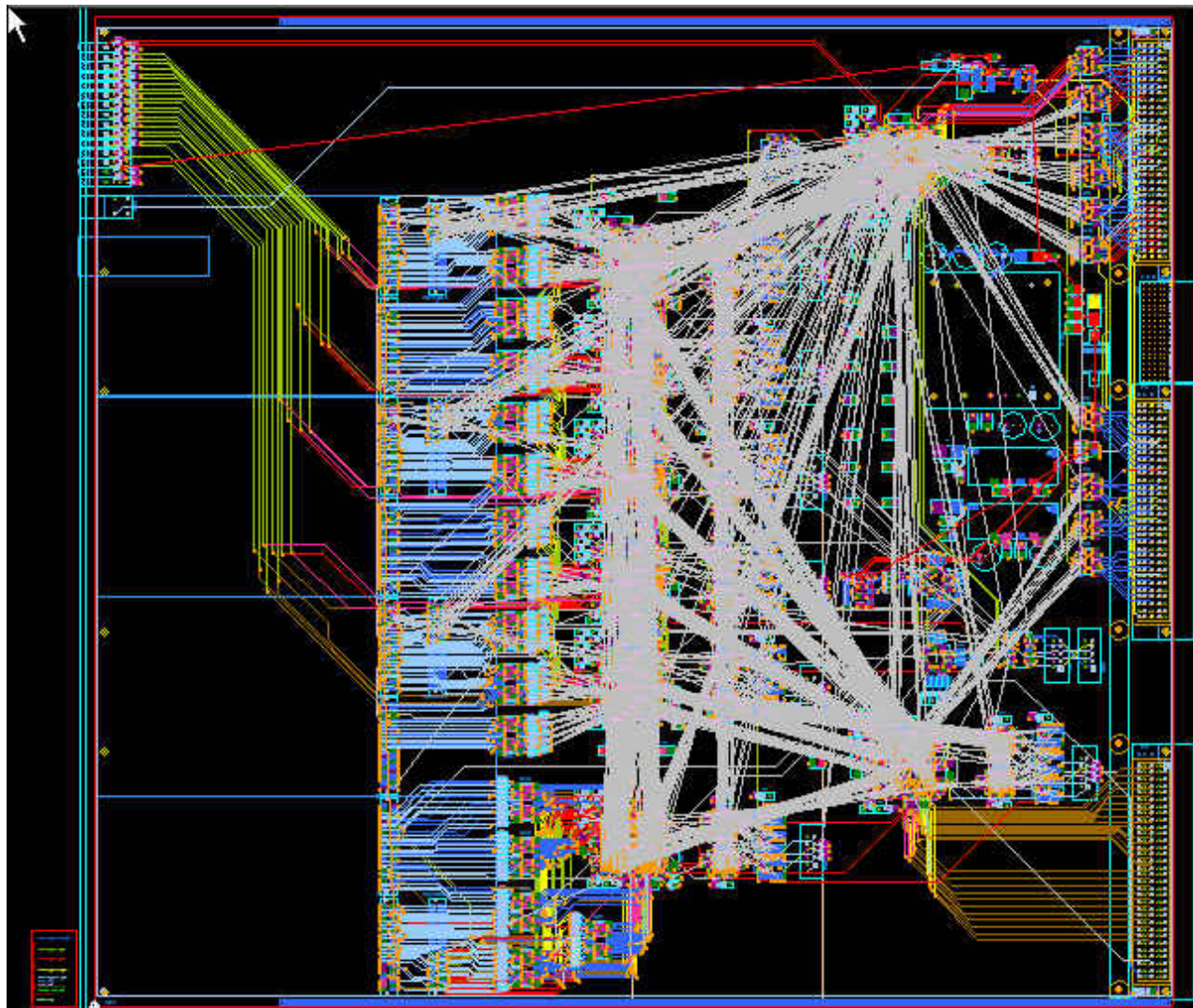
Schedule

Stereo Finder Schedule (set in June'04)

Finish Schematics	**early Sept'04**
Finish Layouts	**early Oct'04**
Preproduction Board under test	**early Dec'04**
Testing complete	**early Mar'05**
Production Readiness Review	**3/21/05**
Production checkout done	**late July'05**